REMARKS

Claims 1 and 14-30 are currently pending in the application. The foregoing separate sheets marked as "Listing of Claims" shows all the claims in the application, with an indication of the current status of each.

The Examiner's indication that claims 1, 19-21, and 24-30 contain allowable subject matter is acknowledged with appreciation.

The Examiner now rejects claims 14-18 and 22-23 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,479,847 to Misewich *et al.* ("Misewich"). Misewich discloses formation of complementary Mott channel layers in order to overcome scaling effects below 100 nm. Misewich uses a laminated structure to create a complementary field effect transistor devices (col. 9, lines 34-39). In detail, Misewich describes formation of a P-type Mott-transition channel layer 602 as shown in Figures 6 and 7. What the Examiner describes as "first 602 (LHS)" on the left hand side of Figure 6 is misconstrued. It should be noted that this "left hand side" is not labeled, which is understandable since it is then removed, as shown in Figure 7. Then an N-type Mott-transition channel layer 801 is formed, as shown in Figures 8 and 9. While both the P-type channel 602 and N-type channel 801 can be grown epitaxially (col. 8, line 11), if so grown they are grown vertically from the substrate.

By contrast, the present invention epitaxially grows its channels not on the substrate but rather upon "a semiconductor region centered between" the channels. In particular, the first epitaxially grown channel is grown upon the "opposite vertical sides" of said semiconductor region. Thus, clearly, the epitaxial growth is horizontal because it is grown from a vertical side. See ¶¶4-6 of the attached Article 132 Declaration of inventor James W. Adkisson.

Further, the Examiner argues that release layer 503 reads on "a semiconductor region centered between the channels", but this layer is not between the channels 602.

Nor does release layer 503 have "opposite vertical sides" upon which an epitaxial channel is in fact grown.

In order to adequately cover the invention, claims 1, 14 and 24 provide different formulations of the method of the invention. For example, both claim1 and claim 14 describe the same channel formation sequence. The first channel is formed on the vertical side surface of a layer (semiconductor region) formed on the substrate, and the layer (semiconductor region) is removed before formation of the second channel. Whereas the description in claim 1 makes explicit the formation of an epitaxial channel on "each of the exposed vertical side surfaces of the layer", and makes explicit that the channel on one side is removed along with the layer before formation of the second channel, claim 14 simply states that a) the first and second epitaxially grown channels are formed, and b) the second channel is formed following c) removal of the semiconductor region centered between he channels and upon whose opposite vertical sides the first channel was grown. Note that neither claim 1 nor claim 14 is explicit about the further processing steps for the second channel, which as those skilled in the art will recognize can be the same as those for forming the first channel (page 12, lines 26-29).

It is respectfully requested that the Examiner reconsider his reliance upon the Misewich reference in the rejection of claim 14, in view of the foregoing indications that Misewich does not support the argument propounded by the Examiner.

However, in order to more promptly advance the prosecution of this case, claim 14 has been amended to more clearly recite the above described aspects of the claim language at issue. In particular, the notion that channels are grown on the vertical sides of the semiconductor region has been moved toward the front of the "forming channels" claim element. Additionally, the "vertical side surfaces extending up from the substrate" attribute of the channels (which, while correct, is not relevant to the claim) has been removed and merged with the "vertical sides" of the

semiconductor region, which also extends "up from the substrate". Further, claim 15 has been amended to more clearly follow the language of claim 14.

As regards claim 15 Misewich is similarly inapposite as a reference. Claim 15 expands upon the channel formation method described in claim 14, providing greater detail and including explicitly the steps for the second channel. As stated in the attached Declaration at ¶¶7-8, nowhere does Misewich teach "an etch stop layer on an exposed side surface of each of the first and second semiconductor lines". Nowhere does Misewich teach "epitaxially growing first and second semiconductor layers on each etch stop layer". Nowhere does Misewich teach "filling areas surrounding the first and second epitaxially grown semiconductor layers and between the source and drain with an oxide fill." Nowhere does Misewich teach "etching a portion of the oxide fill to form an area that defines a gate..." Indeed, there is no "oxide fill" disclosed in Misewich, which means that Misewich cannot disclose etching the fill (Declaration, ¶9), so the ground for rejection of claim 16 is also misplaced.

As to the additional element in claim 17, the Examiner's reference to 602 as being an "...epitaxially grown silicon layer(s)" is not supported anywhere in Misewich, which refers to 602 as a "P-type Mott-transition layer 602 (e.g., La_2CuO_4)" (col 8, line 8-9), which silicon is most certainly not, or more generally an "epitaxially grown cuprate material" (col 1, lines 40-42) , which again, silicon is not. See Declaration, ¶10.

As to the additional element in claim 18, Misewich never discusses silicon dioxide. The Examiner references col 8, lines 16-21, as referring to silicon dioxide. However, this passage does not discuss silicon dioxide. Instead, it discusses only a "gate oxide" layer 603, which in the previous paragraph (col 8 lines 9-10) is discussed as strontium titanate. See Declaration, ¶11.

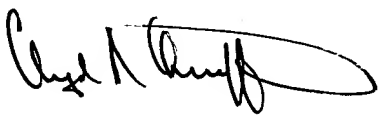
As to claims 22-23, since these depend from claim 14, which has been shown to be allowable, these claims are also allowable.

In view of the foregoing, it is requested that the application be reconsidered, that claims 14-18 and 22-23 be allowed in addition to claims 1 and 24-30, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at 703-787-9400 (fax: 703-787-7557; email: clyde@wcc-ip.com) to discuss any other changes deemed necessary in a telephonic or personal interview.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account 09-0456 (IBM-Burlington).

Respectfully submitted,



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APPENDIX A